

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/146,838
 Priority Filing Date September 3, 1998
 Inventor David L. Dickerson et al.
 Assignee Micron Technology, Inc.
 Priority Group Art Unit 2814
 Priority Examiner A. Mai
 Attorney's Docket No. MI22-1943
 Title: Isolation Region Forming Methods

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING
PRELIMINARY AMENDMENT

In the Specification

At p. 1 before the "Technical Field" section, please insert the following:

RELATED PATENT DATA

This patent resulted from a Continuation Application of U.S. Patent Application
Serial No. 09/146,838, filed September 3, 1998, entitled "Isolation Region Forming
Methods" the disclosure of which is incorporated by reference.

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

There are no amendments to the claims. Claims 1-48 are cancelled herewith and claims 49-68 are added.

-END OF DOCUMENT-

RELATED PATENT DATA

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~~This patent resulted from a Continuation Application of U.S. Patent Application Serial No. 09/146,838, filed September 3, 1998, entitled "Isolation Region Forming Methods" the disclosure of which is incorporated by reference.~~

In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.

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New Claims:

49. (New) A semiconductor construction comprising:
a semiconductor substrate having a trench extending partially therein, the
substrate forming a first sidewall periphery of the trench;
a first masking layer formed over the semiconductor substrate and
comprising a second sidewall periphery of the trench;
a second masking layer formed over the first masking layer and comprising
a third sidewall periphery of the trench; and
wherein the second sidewall periphery is laterally spaced from the first and
third sidewall peripheries, and wherein the third sidewall periphery is laterally
spaced from the first sidewall periphery.

50. (New) The semiconductor construction of claim 49 wherein the construction comprises an intermediate construction of an isolation region.

51. (New) The semiconductor construction of claim 49 wherein the first masking layer comprises silicon dioxide and the second masking layer comprises silicon nitride.

52. (New) The semiconductor construction of claim 49 further comprising an insulative material formed along the first sidewall periphery of the trench.

53. (New) The semiconductor construction of claim 49 further comprising an insulative material partially filling the trench.

54. (New) The semiconductor construction of claim 49 further comprising:

a first insulative material partially filling the trench; and
a second insulative material formed over the first insulative material.

55. (New) A semiconductor construction of an isolation region comprising:

a semiconductor substrate having an opening extending partially therein, the substrate forming a first sidewall periphery of the opening;

a first masking layer formed over the semiconductor substrate and comprising a second sidewall periphery of the opening;

a second masking layer formed over the first masking layer and comprising a third sidewall periphery of the opening; and

wherein the second sidewall periphery is laterally spaced from the first and third sidewall peripheries, and wherein at least a portion of the third sidewall periphery is angled relative an other portion of the third sidewall periphery.

56. (New) The semiconductor construction of claim 55 further comprising an insulative material partially filling the opening.

57. (New) The semiconductor construction of claim 55 wherein the first masking layer comprises silicon dioxide and the second masking layer comprises silicon nitride.

58. (New) The semiconductor construction of claim 55 further comprising an insulative material formed along the first sidewall periphery of the opening.

59. (New) The semiconductor construction of claim 55 further comprising:

- a first insulative material partially filling the opening; and
- a second insulative material formed over the first insulative material.

60. (New) The semiconductor construction of claim 55 wherein the angled portion of the third sidewall periphery forms a facet.

61. (New) The semiconductor construction of claim 55 wherein the construction comprises an intermediate construction of an isolation region.

62. (New) A semiconductor construction of an isolation region comprising:

- a semiconductor substrate having a trench extending partially therein, the substrate forming a first sidewall periphery of the trench;
- a first masking layer formed over the semiconductor substrate and comprising a second sidewall periphery of the trench; and
- a second masking layer formed over the first masking layer and comprising a third sidewall periphery of the trench, the third sidewall periphery comprising a first edge substantially aligned with the first sidewall periphery and a second edge laterally spaced from the first sidewall periphery.

63. The semiconductor construction of claim 62 wherein the construction comprises an intermediate construction of an isolation region.

64. (New) The semiconductor construction of claim 62 wherein the second sidewall periphery is substantially aligned with the first sidewall periphery.

65. (New) The semiconductor construction of claim 62 further comprising an insulative material partially filling the trench.

66. (New) The semiconductor construction of claim 62 wherein the first masking layer comprises silicon dioxide and the second masking layer comprises silicon nitride.

67. (New) The semiconductor construction of claim 62 further comprising an insulative material formed along the first sidewall periphery of the trench.

68. (New) The semiconductor construction of claim 62 further comprising:

a first insulative material partially filling the trench; and

a second insulative material formed over the first insulative material.